A comparison of W-band monolithic resistive mixer architectures

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Abstract **— Three W-band resistive mixer architectures have been designed and their performance compared and contrasted. The mixers were fabricated using 0.1µm gate length InP HEMT technology for improved conversion loss performance compared to GaAs pHEMT. In particular, a state of art 94GHz sub-harmonic resistive mixer is reported with 9.5dB conversion loss when operated with a LO drive level of 2dBm.**

I. INTRODUCTION

Over the last ten years there has been an unprecedented growth in the number of systems that use the mm-wave region of the electromagnetic spectrum. Critical to this growth has been the development of low cost and high performance Monolithic Microwave Integrated Circuits (MMICs) operating in the 30 to 140GHz frequency range. There are well known applications at frequencies such as Ka-band (eg LMDS, MVDS) and V-band (eg ITS, WLAN), however applications are now emerging in W-band which benefit from the high gain, narrow beamwidth antennas or high spatial resolution that is achievable in a compact size at such operating frequencies. Typical applications include passive mm-wave imaging, high-resolution radar, high data rate communications links and radio astronomy systems.

Essential to realising such systems is the development of high performance receiver and transmitter components. For the receive path the availability of small size and highly repeatable mixers is important, particularly in applications where arrays of receiver channels are required.

There are numerous circuit topologies for realising mixers operating in W-band, these include passive approaches, using diodes or cold FETs, and active approaches, using FETs biased in the saturated region of the IV plane. In addition, there are a wide range of physical configurations including single-ended, balanced and double balanced topologies. The chosen circuit approach strongly depends upon system requirements, such as conversion loss, available LO power level, linearity requirements and dc power consumption, along with qualitative factors that assess the degree of risk in achieving a successful design, as illustrated in figure 1.

Receiver sub-systems requiring broadband (75 to 110GHz) and narrowband (94GHz) mixer operation are currently being investigated at QinetiQ for mm-wave imaging and high resolution radar systems respectively. Critical to both applications is the requirement for mixers with high linearity and low LO drive level. Cold FET resistive mixers, based upon InP HEMT technology, are well suited for achieving low intermodulation levels with relatively low LO drive levels. Using InP HEMT technology offers an improvement over a GaAs pHEMT for this type of design in terms of minimum conversion loss and LO power level requirements due to improved channel conductivity and high mobility close to pinch-off [1]. The aim of the work described here was to investigate the performance merits of single ended, balanced and sub-harmonic W-band resistive mixer designs fabricated using InP technology.

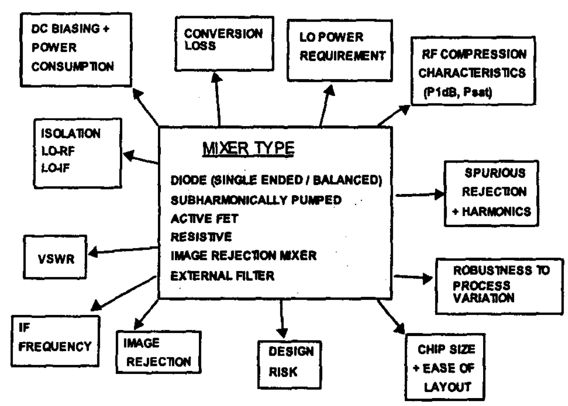

Fig. 1. Typical design factors dictating choice of mixer circuit architecture.

II. CIRCUIT DESCRIPTION

All three MMIC designs were fabricated using the HRL 0.1µm gate length InP HEMT process (ft≥ 150GHz) with a substrate thickness of 50µm. Harmonic balance analysis, using Agilent Series-IV and an in-house derived non-linear model, was used to optimise the performance of each mixer design. In addition, extensive use was made of electromagnetic simulation software (Sonnet EM) to create an accurate passive component model library.

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A. Single ended resistive mixer design

A simplified schematic diagram of the single ended resistive mixer variant is shown in figure 2.

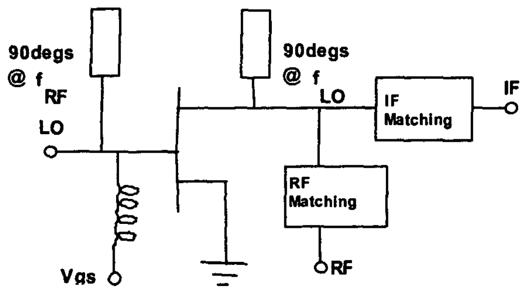

Fig. 2. Single-ended resistive mixer schematic

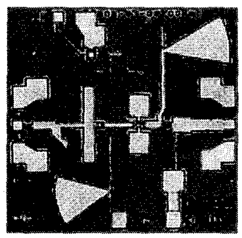

Fig. 3. Photograph of single ended resistive mixer chip

This mixer design is based upon a 2x25μm common-source transistor biased at or near to pinch-off (Vds=0, Vgs=-0.6V). The channel resistance is modulated by applying the LO signal to the gate with matching networks used to inject/extract the RF and IF signals respectively. A simple high-low impedance transformer was used to provide RF matching, with open circuit stubs and series inductive lines used to provide LO matching. The required 11GHz IF was extracted using a low pass filter, realised using a length of high impedance line and a radial line stub. A similar arrangement was used on the gate side for application of bias. Since the drain is unbiased, the transistor gate-drain capacitance (C_{gd}) is relatively large compared to operation in the saturated region, degrading LO-RF isolation for this topology. This can be minimised by adding an inductive resonator between the gate and drain terminals, however this approach was not felt to be practical for W-band operation as C_{gd} can vary significantly due to process variations. A photograph of the single-ended mixer design is given in figure 3, chip size is 1.1mm x 1.175mm.

B. Balanced resistive mixer design

To help overcome the poor LO-RF performance of the single ended resistive mixer, and to achieve broad operating bandwidth, a balanced resistive mixer design was also realised as shown in figure 4 (chip size 1.8mm x 1.1mm). For this design the LO and RF signals are applied in quadrature, using Lange couplers, to two 2x25μm gate width transistors with appropriate RF, LO and IF matching networks. The quadrature couplers allow a significant improvement in LO-RF isolation to be achieved due to phase cancellation of the LO leakage signal at the RF port. The IF signal generated by the mixing elements is in phase and is combined off-chip using an external combiner to give more flexibility in IF operating range.

For this design, problems were encountered in the design of the Lange couplers for operation on 50μm thick InP, since very tight coupling gaps and tracks (2μm) are needed to achieve optimum coupling balance. Therefore it was decided to realise Lange couplers with a non-optimum 4μm track and gap spacing, in order to satisfy minimum line spacing layout rules, with impedance transformers to give an improved port match.

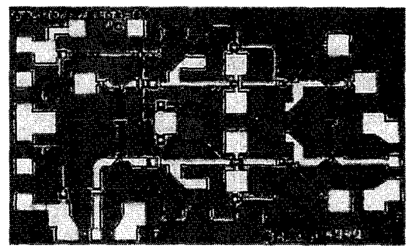

Fig. 4. Photograph of balanced resistive mixer chip

C. Dual-FET sub-harmonic resistive mixer design

The two previous designs are fundamental frequency mixers and require the availability of a W-band LO source. A sub-harmonic mixer design was also examined as this allows the use of a lower frequency LO source which is easier to generate and may offer advantages in terms of available power and phase noise. As with the previous designs a 2x25μm transistor was used as the basic mixing element. This was realised using a 4x25μm transistor cell with the gate manifold divided into two separate halves for application of the LO "+" and "–" signals as shown in figure 5. This approach was adopted, as opposed to having two separate transistor cells, in order to minimise the length of transmission line used to common the drain line output signals. From non-linear simulations it was found that conversion loss was significantly improved by adopting this topology. A Ka-band LO signal is injected through a 180 degree balun, realised using a Wilkinson divider and a half wavelength transmission line, at 41.5GHz, placed on one arm. The mixing elements are therefore driven in anti-phase at the LO frequency and any signal leakage appearing at the RF port is cancelled. At twice the LO frequency, the mixing elements are driven in phase and mixing action occurs with the 94GHz RF signal.

A major difference with this design, compared to the fundamental frequency mixer variants, is that the operating bias voltage had to be chosen to maximise the 2nd harmonic content of the LO waveform in order to minimise conversion loss. The optimum value of gate bias (V_{gs}) was found to be significantly different than for the fundamental mixer designs, with a more negative value required. Apart from the LO signal path, all other matching elements were found to be similar as required for the previous designs. A low pass filter matching network topology, consisting of open circuit stubs and series lengths of high impedance transmission line, was used for LO matching on each transistor gate. A photograph of the sub-harmonic mixer is given in figure 6, chip size is 2.35mm x 1.1mm.

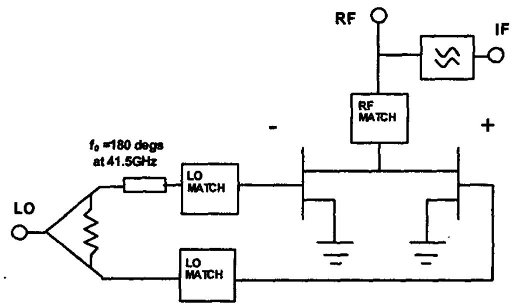

Fig. 5. Schematic of dual-FET sub-harmonic mixer

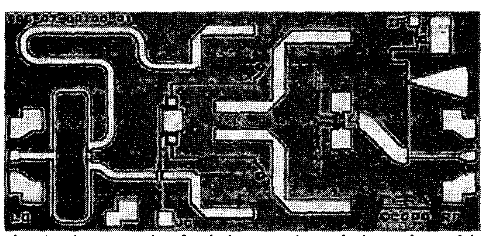

Fig. 6. Photograph of sub-harmonic resistive mixer chip

III. MEASURED RESULTS

Mixer performance was measured on wafer and also in a WR10 waveguide test fixture. Figure 7 shows a comparison of RFOW measured mixer conversion loss versus LO power for the three circuit types.

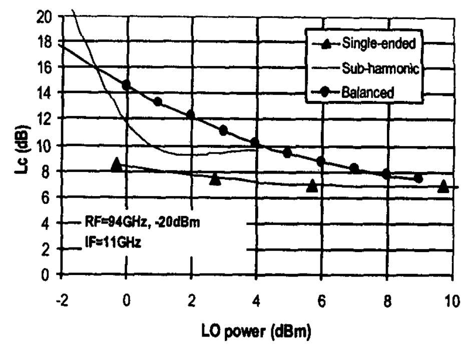

Fig. 7. Measured mixer conversion loss vs LO power

It can be seen that the single ended mixer conversion loss is typically 7 to 8dB and is relatively insensitive to LO drive level over the 0dBm to 8dBm range. The balanced design offers similar conversion loss performance (≈8dB), compared with the single-ended variant, but requires a higher LO power level of +8dBm.The balanced mixer was designed to operate over the whole of W-band and hence there is some degradation in conversion loss performance due to non-optimum LO matching and due to the added insertion loss of the Lange couplers. Conversion loss for the sub-harmonic mixer was 9.5dB with a LO drive level of 2dBm, this level of performance is believed to represent state of art for a monolithic sub-harmonic mixer operating in W-band. A key advantage of the sub-harmonic mixer design is that it can be operated using a standard Ka-band LO source, thus simplifying system level implementation. However, it can clearly be seen that there is a narrower range of LO power levels for optimum operation of the sub-harmonic mixer, compared with the fundamental designs.

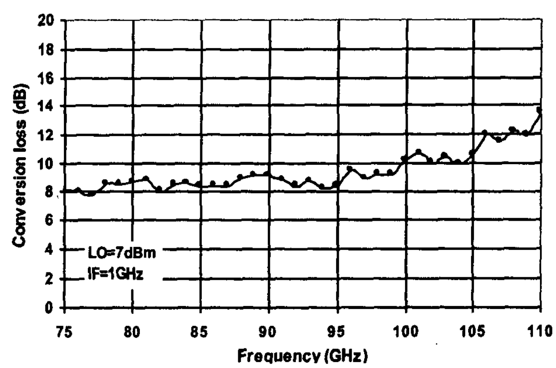

Fig. 8. Conversion loss versus RF frequency for the balanced resistive mixer

The single-ended and sub-harmonic mixer designs both have an RF operating bandwidth of approximately 10%, however the balanced resistive mixer was found to have a conversion loss of better than 12dB over the 75 to 105GHz frequency range, as illustrated in figure 8.

Simulations indicate that the RF P1dB compression point for all three mixer variants should be greater than 4dBm, as illustrated in figure 9. To-date, detailed RF compression measurements have only been performed for the balanced resistive mixer design which was found to have 0.39dB of conversion gain compression for an RF input power of 3dBm. This level of RF input compression, for an LO drive level of 6dBm, is significantly better than can be achieved with standard diode based mixers.

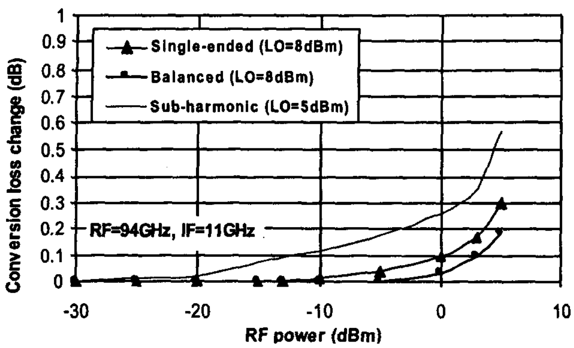

Fig. 9. Simulated RF compression performance

An assessment of mixer isolation performance has also been made. Over the 92 to 96GHz frequency band the LO-RF isolation was found to be 13dB and ≥27dB for the single-ended and balanced mixer variants respectively. For the sub-harmonic mixer design the fundamental LO_1 to RF isolation was >40dB, while the second harmonic LO_2 to RF isolation was >25dB. For all three designs, the LO to IF isolation was better than 35dB (11GHz IF).

V. CONCLUSION

The single-ended resistive mixer design is relatively uncomplicated and hence should give high production yield, it also offers low conversion loss in a small chip area and is insensitive to LO drive level. The main drawback with this topology is its poor LO-RF isolation. It has been shown that the balanced mixer variant offers improved isolation and a broad operating bandwidth at the expense of slightly degraded conversion loss and increased chip size/complexity.

The dual-FET sub-harmonic mixer offers excellent prospects for use in W-band mm-wave receivers as it can be operated using more readily available Ka-band LO sources. State of art conversion loss performance has been demonstrated for this design, 9.5dB, that is comparable to fundamental frequency mixer counterparts. A possible disadvantage of this mixer variant is that its performance is more sensitive to LO drive level than the single-ended or balanced designs. A performance summary for each mixer type is given in Table 1.

ACKNOWLEDGEMENT

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TABLE I

SUMMARY OF RESISTIVE MIXER PERFORMANCE

	Single-ended	Balanced	Sub-harmonic
Chip size (mm)	1.175 x 1.1	1.8 x 1.1	2.35 x 1.1
RF Bandwidth (GHz)	88-100	75-105	88-100
Conversion Loss (dB)	≤8	≤12	≤10
LO power (dBm)	5-6dBm	8dBm	2dBm
LO-RF Isolation (dB) LO-IF Isolation (dB)	13 >35	27 >35	>40 (LO_1) >25 (LO_2) >35
RF 1dB compression (dBm)	>4	>5	>3
Power consumption	zero	zero	zero